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10/516,843	12/03/2004	Jan Hoogerbrugge	NL02 0480 US	7262

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
AYASH, MARWAN	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

MW

Office Action Summary	Application No.	Applicant(s)	
	10/516,843	HOOGERBRUGGE ET AL.	
	Examiner	Art Unit	
	Marwan Ayash	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action has been issued in response to the amendment filed 8/6/07. Claims 1-23 are pending in this application. Applicant's arguments have been carefully considered, but are not persuasive in view of the prior art as applied to a broadest reasonable interpretation of the claims and/or moot in view of new grounds of rejection necessitated by amendment to the claims. The examiner appreciates applicant's effort to distinguish over the cited prior art by more distinctly claiming their invention, however, the claims do not fully overcome the prior art of record. All claims pending in the instant application are rejected and clarification and/or elaboration with respect to why the claims are not in condition for allowance will hereafter be provided (and made distinct via italicizing and/or underlining) in order to efficiently further prosecution.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. **Claims 1, 7, 10, 12, 18, 21 are provisionally rejected** under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 9,1, 3, 10, 4, 6 respectively of copending Application No. 10/495403. Although the conflicting claims are not identical, they are not patentably distinct from each other (see table below).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10/495403	Instant application --- 10/516843
1.Method for writing data elements into a shared FIFO buffer on the basis of semaphore operations, comprising the steps of:	7. Method for writing data elements from a coprocessor into a FIFO memory being in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said method comprising the steps of:
determining if storage space is available in said FIFO buffer to store data elements therein;	checking a first counter, indicating the available room in said FIFO memory, in order to determine whether there is room available in said FIFO memory
b) blocking the input of said FIFO buffer if it has been determined in step a) that no storage space is available in said FIFO buffer ; c) inputting data elements into said FIFO buffer , if it has been determined in step a) that storage space is available in said FIFO buffer ;	issuing a first call for available room in said FIFO memory to said controller until there is room in said FIFO memory; outputting data elements to said FIFO memory;
d) incrementing the count of a write counter, when a data element is input in step c), said count indicating the number of the data elements input in said FIFO buffer ;	decrementing the count of said first counter after a data element has been written into said FIFO memory; incrementing a second counter for counting the number of data elements written into said FIFO memory after a data element has been written into said FIFO memory;
e) performing a first signaling operation when said count of said writer counter has been incremented by L, regardless of a fullness condition of said FIFO buffer.	checking said second counter in order to determine whether a predetermined number N of data elements have been written into said FIFO memory; and issuing a first message that sufficient data elements have been written into said FIFO memory when the count of said second counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory, regardless of a fullness condition of the FIFO.

9. Device for writing data elements into a shared FIFO buffer on the basis of semaphore operations, comprising:	1. Device for writing data elements from a coprocessor into a FIFO memory, in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said device comprising:
first determining means (14) for determining if storage space is available in said FIFO buffer to store data elements therein;	first counter for counting the available room in said FIFO memory;
input blocking means (10) for blocking the input of said FIFO buffer when said first determining means (14) has determined that no storage space is available in said buffer ;	control means for checking said first counter for available room in said FIFO memory [even though blocking means are not explicitly disclosed, method claim 7 includes the step of "issuing a first call for available room in said FIFO memory to said controller until there is room in said FIFO memory"]
input means (11) for inputting data elements into said FIFO buffer , when said first determining means (14) has determined that storage space is available in said FIFO buffer ;	output means for outputting data elements to said FIFO memory;
write counter (12) for incrementing the count thereof when data elements are input in step c), said count indicating the number of the data elements input in said FIFO buffer ;	second counter for counting the number of data elements written into said FIFO memory;
and first signaling means (13) for performing a first signaling operation when said count of said writer counter (12) has been incremented by L, regardless of a fullness condition of said FIFO buffer.	wherein said control means is adapted to issue a first message when the count of said second counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory, regardless of a fullness condition of the FIFO;
3. Method according to claim 1, wherein said step d) comprises the step of incrementing said count of said write counter (12) from a predefined starting count; said method further comprising the steps of: f) determining whether said count of said write counter (12) has reached a predefined first limit L, g) resetting said count of said write counter (12) to said predefined starting point after step f).	10. Method according to claim 7, further comprising to step of: resetting said second counter after issuing said first message.

Claim 10 symmetric to clam 9 only reading instead of writing - and since these claims are symmetric, they are rejected using the same reasoning.	**Claim 12 (symmetric to claim 1) only reading instead of writing**
Claim 4	Claim 18
Claim 6	Claim 21

As instant claims 1, 7, 10, 12, 18, 21 and copending claims 9,1, 3, 10, 4, 6 respectively anticipate each other as detailed above, and as anticipation is the epitome of obviousness, no Graham v. Deere factors are necessary in this instance.

A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (Affirming a holding of obviousness type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
>
> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claims 1,7,12,18 are rejected** under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed [issuing of a message when the count/value of a counter (second and fourth counters) has been incremented to a predetermined number N, regardless of a fullness condition of the FIFO] feature is not supported in the specification in such a manner that would teach one of ordinary skill in the art at the time of the invention how it would be possible to ignore a fullness condition of the buffer when signaling that the buffer is "N entries full". It appears that applicants specification expressly contradicts this limitation (*paragraph 0011 of PGPub 2005/0177659*) wherein applicant discloses that: Two counters are implemented – a first counter for counting available room in the FIFO (therefore inherently being associated with FIFO fullness or lack thereof), and a second counter for counting the number of data elements written into the FIFO (therefore inherently being associated with how full the FIFO is). It is clear from this disclosure that the counters are inherently related to the "fullness" (any degree/level to which the buffer if full) of the FIFO buffer so that one of ordinary skill would be required to perform undue experimentation to overcome the omission of exactly how it would be possible to perform a signaling operation when a count of a read/write counter has been incremented by N (regardless of a fullness condition of said FIFO buffer) when in fact the value of either counter inherently indicates the fullness of the FIFO buffer.

6. **Claims 1,7,12,18 are rejected** under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It appears that one of ordinary skill would need to perform undue experimentation to make the instant invention (in accordance with claim 1 which is representative of all independent claims in the instant application) so that a signaling operation could be triggered upon a counter (which inherently is associated with buffer's fullness) reaching a predetermined value (indicating fullness),

while doing so regardless of a fullness condition of the buffer. Since the counter's value explicitly indicates that the buffer is "N entries/elements/items full", the counter is inherently associated with a fullness condition.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. **Claims 1-23 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Robertson (US Patent # 6,892,253) in view of Bender et al. (US Patent # 5,664,223).

With respect to **independent claims 1, 7, 12, 18** Robertson discloses a device (*Robertson - fig. 4*) for writing data elements from a coprocessor into a FIFO memory, in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said device comprising:

a first counter [*master count 251 (Robertson – abstract)*] for counting the available room in said FIFO memory;

a second counter [*remote count 252 (Robertson – abstract)*] for counting the number of data elements written into said FIFO memory;

control means for checking said first counter for available room in said FIFO memory, for checking said second counter whether a predetermined number N of data elements have been written into said FIFO memory, for decrementing the count of said first counter and for incrementing the count of said second counter after a data element has been written into said FIFO memory [*Robertson - abstract*]; and

output means for outputting data elements to said FIFO memory [*since remote count indicates the number of entries stored in the FIFO buffer (Robertson – abstract, Col 7 lines 48-50), means for outputting/storing data elements into the FIFO are inherent in the disclosure of Robertson's invention; see also fig. 4 of Robertson where the pipeline stages output data to the FIFO buffer 410*];

wherein said control means is adapted to issue a first message when the count of said second counter has reached said predetermined number N [*Upon allocation of N (some variable number) data items into the FIFO buffer, an output signal may be asserted when N is equal to some threshold value (Robertson – Col 5 lines 7-30)*] by incrementing of the count of said second counter after a data element has been written into said FIFO memory [*remote count 252 is incremented upon allocation of data to the FIFO (Robertson - abstract)*], regardless of a fullness condition of the FIFO [*Typically, the threshold value is associated with FIFO fullness since the counter that is incremented upon storage of data into the FIFO inherently indicates how 'full' the FIFO is (1 entry full, 2 entries full... N entries full), and this is the counter that is checked against some threshold value before a signaling/messaging operation is performed (Robertson – abstract, Col 5 lines 7-20). However, since this threshold value is simply a variable that may be set/programmed according to any criteria, it is apparent to one of ordinary skill that the threshold value could be set to any value and not necessarily one associated with 'fullness' per se*];

wherein said control means is adapted to issue a first call for available room in said FIFO memory to said controller [*Column 7 lines 64-67, and/or Col 5 lines 7-30*]; and

wherein said output means is adapted to forward said first message and/or said first call to said controller [*Column 7 lines 64-67, and/or Col 5 lines 7-30*].

Robertson does not **explicitly** disclose the environment in which the invention is implemented - as in the preamble of the instant claim(s) – namely a processor/coprocessor environment. Also, Robertson does not **explicitly** disclose issuing a signal/message upon the second counter reaching a predetermined number of N entries, regardless of a fullness condition of a FIFO. It seems that the main reason why Robertson does not explicitly disclose the latter limitation is because it is inherently self-contradictory since it would be impossible to ignore the fullness condition of the FIFO when issuing a signal based on the value of the second counter seeing as how the second counter explicitly and/or inherently indicates a 'FIFO fullness condition' by indicating that the FIFO is 'N entries full' (1 entry full, 2 entries full...N entries full).

In the same field of endeavor Bender teaches the implementation of a FIFO similar to the one disclosed in Robertson's invention, but in a processor/coprocessor environment (*Bender – Col 2 lines 60-67, Col 4 lines 40-59*) including a controller (*Bender - Col 5 line 19*).

It is noted that the examiner believes the amended limitation (performing a messaging operation based on a counter value regardless of a fullness condition of a FIFO) in the instant claims to be unsupported in the original disclosure in addition to being self-contradictory, however, even as such, a broadest reasonable interpretation of the instant claim(s) remains unpatentable over the examiners stated interpretation of the cited prior art.

Therefore Robertson in view of Bender discloses all limitations of the instant claim(s).

It would have been obvious to one having ordinary skill in the art at the time of the invention to include means for performing a signaling operation when the count of a counter has been incremented by N in the invention of Robertson because it would be advantageous to signal that a fullness/emptiness threshold has been exceeded before the FIFO is actually full/empty since hardware delays and latency properties may not allow a less forgiving implementation to prevent the FIFO from overflowing/underflowing (*Robertson – Col 5 lines 7-20, abstract*). Moreover, it would be advantageous to include means for performing a signaling operation when the count of a counter has been incremented by N to assist with timing of transfer operations into/out from a FIFO memory for the purpose of achieving load balancing in the case of a plurality of FIFO memories (*this*

understanding is supported/evidenced by Myers – US Patent # 6,877,049 – abstract, and/or Myers – US Patent # 2002/0146023 – paragraph 0012-0013).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a FIFO (as part of a decoupling mechanism) in a processor/coprocessor environment in the invention of Robertson as taught by Bender because it would be advantageous to decouple a main processor from certain operations which are cumbersome and which may be (offloaded on/assigned to) a supporting co-processor (*Bender – Col 1 lines 25-37*) thereby effecting more efficient and expedient system operation.

With respect to independent claims 12, 18 Robertson's in view of Bender invention is capable of performing the steps of the claimed method and includes all elements of the claimed device since reading and writing are symmetric operations as is well known by the applicant (paragraph [0006] of applicant's specification). Is well known to one of ordinary skill in the art that reading and writing are symmetric I/O operations such that an exemplary disclosure wherein operations are performed with respect to writing data, would render a symmetric disclosure of operations being performed with respect to reading data an obvious variant.

With respect to **dependent claim 2, 13** as applied to claim 1, 12 above, Robertson in view of Bender discloses said first message indicates that sufficient data elements have been written into said FIFO memory [*Robertson – Col 7 lines 7-30*], [*main processor on the outgoing side will move the packet into its outgoing FIFO and will inform the coprocessor by putting a message into its memory (Bender - Col 10 lines 16-18)*].

With respect to **dependent claims 3, 8, 14, 19** as applied to claims 2, 7, 13, 18 above, Robertson in view of Bender discloses incrementing a write pointer, when data elements were output to said FIFO memory [*When data is put into the FIFO, the tail pointer is incremented and when data is taken out of the FIFO the head pointer is incremented (Bender - Col 10 lines 39-42)*].

With respect to **dependent claims 4, 9, 15, 20** as applied to claims 3, 8, 14, 19 above, Robertson in view of Bender discloses performing a wrap-around test after said write pointer was incremented [*check to see if the tail pointer (+2) is not equal to the header pointer (Bender - Col 11 lines 4-6)*].

With respect to **dependent claims 5, 10, 16, 21** as applied to claims 2, 7, 13, 18 above, Robertson in view of Bender discloses resetting said second counter after issuing said first message [*Robertson – Col 7 lines 47-62*], [*a reset device, operatively coupled to said output of the counting mechanism, for resetting the adaptor; and a reset transmitting device, operatively coupled between the reset device and the main processor for transmitting the reset condition of the adaptor to the main processor (Bender - Col 3 lines 35-40)*].

With respect to **dependent claims 6, 11, 17, 22** as applied to claims 1, 7, 13, 18 above, Robertson in view of Bender discloses issuing said first call for available room in said FIFO memory to said controller before said count of said first counter becomes zero [*Robertson – Col 5 lines 7-30*], [*it first polls the head pointer in its local memory and compares it with its cached value of the tail pointer to determine if there is space in the outgoing FIFO... checks to see if the tail pointer (+2) is not equal to the header pointer (Bender - Col 11 lines 2-6); If it is full, local polling occurs at the coprocessor. While there is polling occurring, the main processor can send a new "receive head" through the adaptor to thereby update the "receive head" in the coprocessor 22. (Bender - Col 13 lines 10-14). Note that issuing the call before the count of first counter becomes zero is understood to be functionally equivalent to setting a predetermined threshold value which indicates an almost full state for the FIFO queue and issuing the call based on the counter or pointer reaching that value*].

With respect to **dependent claim 23** as applied to claim 1 above Robertson in view of Bender discloses a Multiprocessing computer system, comprising: a FIFO memory; at least one coprocessor; a controller, a device for writing according to claim 1 [*See rejection of claim 1 above*].

Response to Arguments

Applicant's arguments filed 8/6/07 have been fully considered but are moot in view of the new ground(s) of rejection. The rejections of claims 1-23 are maintained.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. When responding to the office action, applicants are advised to clearly point out the patentable novelty which they think the claims present in view of the state of the art disclosed by the references cited or the objections made. Applicants must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c). In addition, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner in locating the appropriate paragraphs. **Any new claims and/or limitations should be accompanied by a reference as to where the new claims and/or limitations are supported in the original disclosure**.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marwan Ayash whose telephone number is 571-270-1179. The examiner can normally be reached on Mon-Fri 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Marwan Ayash -- Examiner -- Art Unit 2185

8/21/07

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100